



Job Title: Mask Designer / IC Layout Engineer– Imagers

Description:

This position is located in Panavision Imaging, LLC, New York design center and will focus on the development of CMOS image sensor products. Panavision Imaging sensor products are targeted at consumer applications such as bar code, machine vision and high-performance digital-still and video cameras. Product development will focus on expanding our current product offerings.

Job Requirements:

The qualified applicant will demonstrate experience in the custom analog layout of integrated circuits including the ability to place and route active and passive devices. This includes the ability to plan the placement of major circuit components in an overall physical design and an understanding of how the physical layout can affect circuit performance of circuits like amplifiers, switches, digital blocks and other imager related functional blocks.

The applicant must have a basic understanding of both digital and analog electrical circuits, be able to read electrical schematics and netlists, and be able to perform layout vs. schematic (LVS), design rule checks (DRC), electrical rule checks (ERC), ESD and latch-up checks, and antenna rule checks using the Tanner and Calibre verification tools. An understanding of semiconductor processes like CMOS is desirable.

Knowledge of SKILL, Perl or C++ desirable but not required.

Required Skills:

Tanner Tools,
Calibre verification
Analog/ Mixed Layout,
Tanner, Mentor,

Desired Skills:

Knowledge of SKILL, Perl or C++ desirable but not required.

Minimum Requirements:

5 years minimum in CMOS Mixed Signal layout, Strong knowledge of transistor-level full custom CMOS analog circuit layout and verification. Imager layout experience a plus.